REMARKS

Attached hereto is an Excess Claim Fee letter and fee for excess total claims.

It is noted that, notwithstanding any claim amendments made herein, Applicant's intent is to encompass equivalents of all claim elements, even if amended herein or later during prosecution.

Claims 1-3 and 5-22 are all of the claims pending in the present Application. Claim 4 is canceled above and new claims 20-22 have been added. Claims 1-7 stand rejected under 35 USC §103(a) as unpatentable over US Patent 6,054,863 to Morrison et al, further in view of US Patent 6,288, 561 to Leedy. Claims 14-18 stand rejected under 35 USC §103(a) as unpatentable over US Patent 6,201,383 to Lo et al, further in view of Leedy. Claim 8 stands rejected under 35 USC §103(a) as unpatentable over Morrison/Leedy, further in view of US Patent 5,438,272 to Craig et al. Claims 9-13 and 19 stand rejected under 35 USC §103(a) as unpatentable over Lo/Leedy, and further in view of US Patent 5,420,500 to Kerschner.

These rejections are respectfully traversed in view of the following discussion.

I. THE CLAIMED INVENTION

As described and claimed, e.g., by claim 1, the present invention is directed to an electronic circuit wiring interconnect package test and repair apparatus including at least one wiring analyzer to locate shorts between conductors on a surface of or embedded in a carrier substrate. The carrier substrate includes only conductors at the time of testing. These conductors are intended to interconnect components *that are not yet mounted* on the carrier substrate. A current source provides current sufficient to remove the shorts.

A cluster probe, comprising a plurality of probes, contacts the conductors in a manner controlled by the wiring analyzer. .

No cited prior art reference defines a test/repair apparatus for a wiring interconnect package, i.e., a carrier substrate having conductors to interconnect electronic components, wherein the carrier substrate is totally devoid of any such components at the time of testing as defined by the apparatus and process of the present invention.

Advantages of the present invention is that cost and time is considerably reduced for the manufacture of wiring interconnect packages. Indeed, in at least one version of the present invention, a completely automated check of a substrate can be made by making a single contact by the cluster probe to the substrate.

That is, the present invention provides the capability in which a substrate is contacted one time with the cluster probe. The wiring analyzer will check for short and open circuits by systematically taking measurements through predetermined probes of the cluster probe. Without even moving the cluster probe, one or more attempts can then be made to systematically remove any short circuit(s) located by the analyzer, including the optional test of an overvoltage stress test. The substrate is then again re-tested in its entirety, again without moving the cluster probe.

By this novel approach, a substrate can be thoroughly checked out and repaired in a single test apparatus and eliminates even the time-consuming necessity of relocating probes to different locations on the substrate.

II. THE PRIOR ART REJECTIONS

Applicants again submit, prior to proceeding to appeal, that the Examiner continues to incorrectly apply the evaluation guidelines of MPEP §2143. The Examiner seems not to yet understand the significance of the present invention or the difference between the art of testing carriers versus the art of performing a final functional test of a complete IC. As described on pages 1 and 2 of the specification and as confirmed by various references cited by the Examiner, the current state of the art for wiring interconnect package testing is that the repair of these packages requires a separate repair apparatus from that used to test for shorts or other defects.

The present invention overcomes this problem of the art, thereby providing the advantage of saving time and cost for the manufacture of these wiring interconnect packages. The rejection of record still fails to provide a single reference that combines testing and repair of wiring interconnect packages in a single apparatus, let alone an apparatus that allows a

wiring interconnect package to be tested and repaired without even once moving the contact probes.

In general, the rejection of record continues to ignore the difference of a functional test for a complete integrated circuit compared to checking out a carrier substrate devoid of functional components for short circuits. In so doing, the Examiner takes the concept of "functional test" out of context and then combines this concept as an abstraction into a new environment that is not suggested by the prior art and which combination is inherently incompatible. Such combination is improper under several guidelines of MPEP §2143, as identified below.

The Rejection based on Morrison/Leedy

The Examiner alleges that US Patent 6,054,863 to Morrison et al, further in view of US Patent 6,288, 561 to Leedy, renders obvious claims 1-7. The Examiner correctly concedes that Morrison fails to teach or suggest a current source for providing current sufficient to remove short circuits located by the wiring analyzer. To overcome this deficiency, the Examiner relies on Leedy.

According to the Examiner, one of ordinary skill in the art would have been motivated to "incorporate the current source of Leedy into the apparatus of Morrison et al. for the purpose [of] reducing the number of steps and therefore time needed to produce functional boards that are free of defects (column 2, lines 4-9)."

Applicants again submit that the rejection of record meets the initial burden of a *prima facie* rejection for the following reasons.

First, to form a motivation to combine Leedy with Morrison, the Examiner clearly lifts words out of context, thereby selectively removing the very language that clearly demonstrates that no suggestion is made in Leedy to incorporate features therein with a test apparatus for circuit boards of Morrison. That is, line 9 of column 2 of Leedy clearly limits the discussion therein to "IC burn-in, testing, repairing and/or programming". Nowhere does Leedy even suggest that any techniques discussed therein could be extended to other arts. It is the Examiner who designates this IC apparatus as appropriate to incorporate into the art of testing circuit boards.

As indicated in US Patent 5,290, 986 to Colon et al., previously provided by Applicants in the IDS filed April 10, 2001, as prior art potentially related to the present invention, repair of carrier substrates, such as those based on glass ceramics substrates, have unique problems not found in IC testing. At least two problems discussed in Colon (see lines 20-37 of column 4) differentiate the art of testing glass ceramic substrates from the art of testing IC's because different materials and a different scale of conductor size are involved in the two separate arts. That is, in the carrier substrates, there is the potential of cracking of glass and failure of the burned out metal to be drawn back to the parent conductor lines during attempts to eliminate short circuit.

Second, a major difference in the two arts occurs because ICs can inherently be "functionally" tested only after the component devices have been fabricated on the wafer. That is, ICs typically have the interconnection layers applied only **after** the component devices have been fabricated. There is no stage in IC manufacturing that corresponds to the testing of a carrier substrate having conductors but otherwise devoid of components. The Examiner attempts to make the concept of functional testing of ICs as an abstract idea to be imported into other electronic arts. In doing so, the Examiner violates the following guidelines from MPEP §2143.01:

- "The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination." (Emphasis in MPEP and not by Applicants)

- "The proposed modification cannot render the prior art unsatisfactory for its intended purpose." (In the proposed combination, Morrison would no longer function as a test for circuit boards devoid of components as described at lines 21-23 of column 4, since the functional test of Leedy requires that components be present, as clearly described at lines 49-52 of column 7.)

- "The proposed modification cannot change the principle of operation of a reference." (By incorporating the Leedy functional test requiring that components be present, the principle of operation of the test apparatus of Morrison would be changed from the timing circuit measurement circuits into a circuit requiring that circuit functions be analyzed. As just mentioned above, as well as at lines 49-52 of column 1, Morrison relies upon a testing

principle in which unpopulated circuit boards are assumed, rather than an analysis of circuit functions.

Essentially, as described at lines 49-552 of Leedy, for Leedy to be combined into Morrison, the timing circuits of Morrison would have be totally replaced by a computer that "supplies the control signals, receives data signals back from the probing points, and analyzes the data to determine which ICs are functional on the wafer." Stated slightly differently, the technique in Leedy is totally incompatible with the technique in Morrison.

Finally, Morrison's principle of operation is that of testing only. The urged combination changes this principle of operation into a principle of testing and repair.)

Third, even if Leedy were to be combined with Morrison, the combination would still fail to provide **all** the limitations of the independent claims (see MPEP §2143.03: "All claim limitations must be taught or suggested"). By incorporating a functional test technique that analyzes whether an IC is functional, the urged combination inherently ignores the clear language of the claims that the electronic circuit wiring interconnect package be devoid of components. That is, the process of logically combining Leedy with Morrison inherently defeats the original characteristic of Morrison in which the circuit board was unpopulated.

The advantage of the present invention over Morrison is that a single apparatus can not only be used for both testing and repair of electronic circuit wiring interconnect packages, but also, by using a cluster probe to make contact with the wiring interconnect package, the cluster probe does not have to be moved even one time during the testing and repair. Significant savings in both cost and time is achievable by the present invention in comparison with the conventional techniques exemplified by Morrison.

Hence, turning to the clear language of the claims, there is no teaching or suggestion in Morrison of: "... a current source to provide current sufficient to remove said shorts", as required by claim 1.

Additionally, relative to the rejection for claim 2, Applicants again submit that nowhere does either Morrison or Leedy even suggest using two wiring analyzers.

Relative to the rejection for claim 5, Applicants again submit that the description at lines 60-64 of column 6 of Leedy that "... high voltage of current can be provided between the

appropriate probe points to open up a conducting path ..." is not at all a high voltage stress test.

The Rejection based on Lo/Leedy

The Examiner alleges that US Patent 6,201,383 to Lo et al, further in view of Leedy, renders obvious claims 14-18. The Examiner concedes that Lo fails to teach or suggest the current source for removal of shorts but considers the description at lines 54-57 of column 6 as motivation to combine Leedy with Lo. That is, the Examiner alleges that one would be motivated "... to incorporate the current source of Leedy in the apparatus of Lo et al. for the purpose of removing shorts and repairing electronic circuits since it is stated by Lo et al. that "it is desirable to determine which networks are shorted together, so that the circuit can be repaired" (column 6, lines 54-56)."

Applicants disagree, for many or all of the reasons identified above for the rejection based on Morrison.

First, it is assumed that the term "networks" used in Lo are interpreted as being conductors on/in a substrate devoid of components, since, otherwise, Lo cannot be considered in the same art as the present invention, any more than Leedy could be.

Second, Applicants submit that the statement relied upon by the Examiner ("... so that the circuit can be repaired...") actually confirms the description of the state of the art for wiring interconnect package testing, as described on pages 1 and 2 of the specification, at the time of the present invention as being well understood that the repair of these packages requires a separate repair process and apparatus from that used to test for shorts or other defects. Therefore, rather than making a suggestion to incorporate a feature of Leedy into Lo, as the Examiner attempts to interpret this description, this statement in Lo actually makes a simple statement that clearly demonstrates the state of the art at the time of the invention. By providing the advantage of saving time and cost for the manufacture of these wiring interconnect packages, the present invention clearly provides an improvement in the state of the art, as described by this statement in Lo.

Third, similar to the argument above for the rejection based on Morrison, the rejection based on Lo/Leedy violates the guidelines of MPEP from MPEP §2143.01:

- "The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination." (Emphasis in MPEP)

- "The proposed modification cannot render the prior art unsatisfactory for its intended purpose." (In the proposed combination, Lo would no longer function as a test for circuit boards devoid of components as Lo is presumed to be interpreted, since the functional test of Leedy requires that components be present, as clearly described at lines 49-52 of column 7.)

- "The proposed modification cannot change the principle of operation of a reference." (By incorporating the Leedy functional test requiring that components be present, the principle of operation of the test apparatus of Lo would be changed, from the simple technique of providing voltage to one of the networks and sensing which, if any, other networks have current flow, to become a principle of operation based on analyzing circuit function.

That is, similar to the urged combination between Morrison/Leedy, for Leedy to be combined into Lo, the test circuits in Lo would have be totally replaced by a computer that "supplies the control signals, receives data signals back from the probing points, and analyzes the data to determine which ICs are functional on the wafer." Finally, Lo's principle of operation is that of testing only. The urged combination changes this principle of operation into a principle of testing and repair.)

Fourth, even if Leedy were to be combined with Lo, the combination would still fail to provide **all** the limitations of the independent claims (see MPEP §2143.03: "All claim limitations must be taught or suggested"). By incorporating a functional test technique that analyzes whether an IC is functional, the urged combination inherently ignores the clear language of the claims that the electronic circuit wiring interconnect package be devoid of components. That is, the process of logically combining Leedy with Lo inherently defeats the original characteristic of Lo in which the circuit board was unpopulated.

Hence, turning to the clear language of the claims, there is no teaching or suggestion in Lo of: "... a current source to provide current sufficient to remove said shorts", as required by claim 14.

Additionally, relative to the rejection for claim 15, Applicants again submit that nowhere does either Lo or Leedy even suggest using two wiring analyzers.

Relative to the rejection for claim 17, Applicants again submit that the description at lines 60-64 of column 6 of Leedy that "... high voltage of current can be provided between the appropriate probe points to open up a conducting path ..." is not at all a high voltage stress test.

An identical response applies for the rejection of claims 9-13 and 19, as based on improperly combining Lo and Leedy, since Kerschner is introduced for purpose of demonstrating the location of unintended open circuits.

The Rejection based on Morrison/Craig et al.

Relative to the rejection currently of record for claim 8, the Examiner concedes that Lo fails to teach or suggest the claimed feature that multiple attempts are made to remove shorts and introduces Craig, pointing to wording in claim 4(2).

However, a fair reading of these lines indicates no relation whatsoever to the claimed subject matter. That is, the process described in these lines concerns the successive probing to determine whether a short circuit exists. It has nothing whatsoever to do with attempting to remove an identified short circuit nor with making multiple attempts.

For this reason alone, the claimed invention is fully patentable over the cited references.

For any of the reasons stated above, the claimed invention is fully patentable over the cited references.

Further, the other prior art of record has been reviewed, but it too, even in combination with the Morisson, Lo, Leedy, Kerschner, or Craig, fails to teach or suggest the claimed invention.

IV. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 1-3 and 5-22, all the claims presently pending in the application, are patentably distinct over the prior art of record and

are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Assignee's Deposit Account No. 09-0458.

Respectfully Submitted,

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